AMENDMENTS TO THE CLAIMS

In accordance with 37 C.F.R. §1.121(c), please amend the claims as indicated in marked-up form below, where additions are underlined, deletions are struck through, and new claims are presented without markings.

1. (Currently Amended) A microelectronic device comprising:

a package substrate having a first side and an opposing second side;

a package connector at the second side of the package substrate and a board coupled to the package connector;

a microprocessor adjacent to the first side of the package substrate; and

a memory device adjacent to the second side of the package substrate, wherein the package substrate is electrically coupled to at least one of the microprocessor and the memory device and wherein the memory device is located in a cavity defined by the package connector, the package substrate, and the board.

2. (Original) The apparatus of Claim 1, further comprising a memory controller electrically coupled to the memory device.

3. (Original) The apparatus of Claim 1, further comprising a thin film capacitor integral to the substrate.

4. (Currently Amended) The apparatus of Claim 1, the ~~second die~~ memory device disposed on a land side of the package substrate.

5. (Original) The apparatus of Claim 1, further comprising a third die including a second microprocessor, a fourth die including a third microprocessor, and a fifth die including a fourth microprocessor.

6. (Currently Amended) The apparatus of Claim 5, the ~~second die~~ memory device electrically coupled by one selected from the group including a wirebond electrical interconnect, a flip-chip ball grid array electrical interconnect, a lead frame interconnect, and a combination thereof.

7. (Original) The apparatus of claim 1 further comprising a die including one selected from the group including a memory device, a memory controller, an application specific integrated circuit (ASIC), a graphics processor, a signal processor, a radio transceiver, and a combination thereof.

8. (Original) The memory device of Claim 7 further comprising a fourth level cache.

9. (Currently Amended) The apparatus of Claim 1, the package further including an integrated heat spreader thermally coupled to one or more of the ~~die~~ microprocessor and the memory device.

10-17. (Canceled)

18. (Withdrawn) A system comprising:

a package including an integrated circuit disposed on two or more electrically coupled die, the first die including a microprocessor and the second die including a memory device;

a system memory bus coupled to the microprocessor;

a package substrate electrically coupled to at least one of the die; and

a mass storage device coupled to the package, wherein the memory device has a speed that exceeds a speed of the system memory bus.

19. (Withdrawn) The system of Claim 18 wherein the memory device further comprises a fourth level cache.

20. (Withdrawn) The system of claim 18, further comprising:

a dynamic random access memory coupled to the integrated circuit; and

an input/output interface coupled to the integrated circuit.

21. (Withdrawn) The system of claim 20, wherein the input/output interface comprises a networking interface.

22. (Withdrawn) The system of claim 18, wherein the system is a selected one of a group comprising a set-top box, a media-center personal computer, a digital versatile disk player, a server, a personal computer, a mobile personal computer, a network router, and a network switching device.

23. (Withdrawn) The system of claim 18, the memory device disposed in a recess formed by a land grid array socket, the package electrically coupled to the land grid array connector.

24. (Withdrawn) The system of claim 23, the land grid array connector coupled to a printed circuit board assembly capable of further coupling to a motherboard.

25. (Previously Presented) The microelectronic device of claim 8, wherein the fourth level cache has a capacity ranging between approximately 500 megabytes and approximately 1 gigabyte.

26. (Previously Presented) The microelectronic device of claim 25 further comprising a system memory bus coupled to the microprocessor, wherein the fourth level cache has a speed greater than a speed of the system memory bus.

27. (Currently Amended) The microelectronic device of claim 1 ~~further comprising~~ wherein the package connector comprises a land grid array connector coupled to the package substrate.

28. (Currently Amended) The microelectronic device of claim 1 ~~further comprising~~ wherein the package connector comprises a pin grid array connector coupled to the package substrate.

29. (Currently Amended) A microelectronic device comprising:

a package substrate;

a package connector coupled to the package substrate and a board coupled to the package connector;

a microprocessor coupled to the package substrate; and

a memory device coupled to the package substrate, wherein the memory device comprises a fourth level cache and wherein the memory device is located in a cavity defined by the package connector, the package substrate, and the board.

30. (Previously Presented) The microelectronic device of claim 29 wherein:

the fourth level cache has a capacity ranging between approximately 500 megabytes and approximately 1 gigabyte.

31. (Previously Presented) The microelectronic device of claim 30 further comprising:

a third level cache and a system memory bus,

wherein:

the fourth level cache has a speed greater than a speed of the system memory bus; and

the capacity of the fourth level cache is greater than a capacity of the third level cache.

32. (Currently Amended) The microelectronic device of claim 31 ~~further comprising~~ wherein the package connector is one of a land grid array connector and a pin grid array connector ~~coupled to the package substrate~~.